

What is claimed is:

1. A method of manufacturing a semiconductor integrated circuit comprising the steps of:

disposing an upper interlayer on a stopper film layered on a surface of a lower interlayer film
5 including a metal wiring embedded in a concave formed therein;

forming a via hole extending from the surface of said upper interlayer film to the surface of said stopper film at an opposite position to said metal
10 wiring;

forming an organic film on the surface of said upper interlayer film and embedding the material of said
20 organic film in said via hole, and forming a resist mask with an opening to communicate with the opening of said
15 via hole on the surface of said organic film;

plasma etching said organic film formed on the surface of said upper interlayer film through the opening in said resist mask in an atmosphere of an etching gas and an inert gas;

simultaneously plasma etching said upper interlayer film exposed by plasma etching said organic film and the material of said organic film embedded in said via hole to a predetermined depth which does not reach said stopper film in an atmosphere of an etching
25 gas and an inert gas with the etching rate for said

sub
A17
organic film with said etching gas higher than the
etching rate for said upper interlayer film with said
etching gas; and

removing the material of said organic film
30 remaining in said via hole positioned at the bottom of a
concave groove formed by said plasma etching and etching
said stopper film positioned at the bottom of said via
hole from which the material of said organic film is
removed to expose said metal wiring.

2. A method of manufacturing a semiconductor
integrated circuit comprising the steps of:

disposing an upper interlayer on a stopper
film layered on a surface of a lower interlayer film
5 including a metal wiring embedded in a concave formed
therein;

forming a via hole extending from the surface
of said upper interlayer film to the surface of said
stopper film at an opposite position to said metal
10 wiring;

forming an organic film on the surface of said
upper interlayer film and embedding the material of said
organic film in said via hole, and forming a resist mask
with an opening to communicate with the opening of said
15 via hole on the surface of said organic film;

plasma etching said organic film formed on the

surface of said upper interlayer film through the opening
in said resist mask in an atmosphere of an etching gas
including a molecular structure which produces no
20 deposition and an inert gas;

simultaneously plasma etching said upper
interlayer film exposed by plasma etching said organic
film and the material of said organic film embedded in
said via hole to a predetermined depth which does not
25 reach said stopper film in an atmosphere of an etching
gas and an inert gas; and

removing the material of said organic film
remaining in said via hole positioned at the bottom of a
concave groove formed by said plasma etching and etching
30 said stopper film positioned at the bottom of said via
hole from which the material of said organic film is
removed to expose said metal wiring.

3. The method of manufacturing a semiconductor
integrated circuit according to claim 1, wherein said
etching gas includes atoms of fluorine and atoms of
carbon contained in a molecular structure, the number of
5 the atoms of fluorine being three times or more than the
number of the atoms of carbon.

4. The method of manufacturing a semiconductor
integrated circuit according to claim 3, wherein said

4-17
A17
etching gas comprises "CF₄".

5. The method of manufacturing a semiconductor integrated circuit according to claim 3, wherein said etching gas comprises "C₂F₆".

6. The method of manufacturing a semiconductor integrated circuit according to claim 2, wherein said etching gas includes atoms of fluorine and atoms of carbon contained in a molecular structure, the number of the atoms of fluorine being three times or more than the number of the atoms of carbon.

7. The method of manufacturing a semiconductor integrated circuit according to claim 6, wherein said etching gas comprises "CF₄".

8. The method of manufacturing a semiconductor integrated circuit according to claim 6, wherein said etching gas comprises "C₂F₆".

9. The method of manufacturing a semiconductor integrated circuit according to claim 1, wherein a pressure in said atmosphere is "100 [mToll]" or higher.

10. The method of manufacturing a semiconductor

integrated circuit according to claim 2, wherein a pressure in said atmosphere is "100 [mToll]" or higher.

11. A semiconductor integrated circuit comprising a concave groove formed to extend from a surface of an interlayer film including a metal wiring embedded therein to a predetermined depth, a via hole formed at the bottom
5 of said concave groove, said metal wiring being exposed at the bottom of said via hole, said semiconductor integrated circuit being manufactured by the manufacturing method according to claim 1.

12. A semiconductor integrated circuit comprising a concave groove formed to extend from a surface of an interlayer film including a metal wiring embedded therein to a predetermined depth, a via hole formed at the bottom
5 of said concave groove, said metal wiring being exposed at the bottom of said via hole, said semiconductor integrated circuit being manufactured by the manufacturing method according to claim 2.